PW050N06HSL

Perfect MOS N-MOSFET 60V, 4.2mΩ, 54A

重庆平伟实业股份有限公司

Features

- Uses PingWei advanced PerfectMOS technology
- Extremely low on-resistance $R_{DS(on)}$
- Excellent $Q_g x R_{DS(on)}$ product(FOM)
- Excellent Low Ciss
- Qualified according to JEDEC criteria

Benefits

- High robustness and reliability
- Increases maximum current capability
- Low power loss, high power density
- Easy paralleling

Applications

- Synchronous Rectification for AC/DC Quick Charger
- Battery management
- UPS (Uninterrupible Power Supplies)

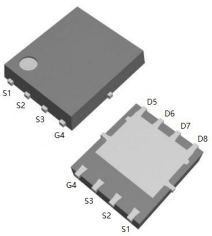
100% DVDS Tested

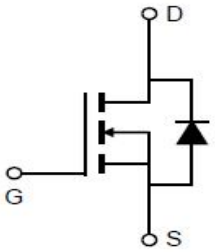
100% AvalancheTested

Product Summary

V_{DS}	60V
$R_{DS(on)@10V\ typ}$	4.2mΩ
$R_{DS(on)@4.5V\ typ}$	5.8mΩ
I_D	54A

DFN3x3





Package Marking and Ordering Information

Part #	Marking	Package	Packing	Reel Size	Tape Width	Qty
PW050N06HSL	050N06HSL	DFN3*3	Tape&Reel	13 inches	12mm	5000pcs

Absolute Maximum Ratings

Parameter	**Symbol**	**Value**	**Unit**
Drain-source voltage	V_{DS}	60	V
Continuous drain current			
T_C = 25°C (Silicon limit)	I_D	73	A
T_C = 25°C (Package limit)		54	
T_C = 100°C (Silicon limit)		46	
Ta = 25°C		12	
Pulsed drain current (T_C = 25°C)	$I_{D\ pulse}$	216	A
Avalanche energy, single pulse (L=0.5mH)	E_{AS}	56	mJ
Gate-Source voltage	V_{GS}	±20	V
Power dissipation			
T_C = 25°C	P_{tot}	45	W
Ta = 25°C		1.3	
Operating junction and storage temperature	T_j , T_{stg}	-55...+150	°C
Soldering temperature, wave soldering only allowed at leads (1.6mm from case for 10s)	Tsold	260	°C

Thermal Resistance

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Thermal resistance, junction – case.	RthJC	-	-	2.8	°C/W	-
Thermal resistance, junction - ambient(min. footprint)	RthJA	-	-	98	°C/W	-

Electrical Characteristic (at Tj = 25 °C, unless otherwise specified)

Parameter	**Symbol**	**Value**			**Unit**	**Test Condition**
		min.	**typ.**	**max.**		
Static Characteristic						
Drain-source breakdown voltage	BV_{DSS}	60	-	-	V	V_{GS}=0V, I_D=250uA
Gate threshold voltage	$V_{GS(th)}$	1.2	-	2.5	V	V_{DS}=V_{GS},I_D=250uA
Zero gate voltage drain current	I_{DSS}	- -	- -	1 100	μA	V_{DS}=60V,V_{GS}=0V T_j=25°C T_j=150°C
Gate-source leakage current	I_{GSS}	-	-	±100	nA	V_{GS}=±20V,V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	-	4.2	5.0	mΩ	Vgs=10V,Id=30A
		-	5.8	7.5		Vgs=4.5V,Id=30A
Transconductance	g_{fs}	-	56	-	S	V_{DS}=5V,I_D=20A
Dynamic Characteristic						
Input Capacitance	C_{iss}	-	1927	-	pF	V_{GS}=0V, V_{DS}=30V, f=1MHz
Output Capacitance	C_{oss}	-	421	-		
Reverse Transfer Capacitance	C_{rss}	-	39	-		
Gate Total Charge	Q_G	-	35	-	nC	Vds=30V,Id=50A ,Vgs=10V
Gate-Source charge	Q_{gs}	-	9.3	-		
Gate-Drain charge	Q_{gd}	-	6.4	-		
Turn-on delay time	$t_{d(on)}$	-	9.5	-	ns	V_{GS}=10V, V_{DD}=30V, R_{G_ext}=1.6Ω,Id=50A
Rise time	t_r	-	43.6	-		
Turn-off delay time	$t_{d(off)}$	-	32.4	-		
Fall time	t_f	-	13.5	-		
Gate resistance	R_G	-	2.3	-	Ω	V_{GS}=0V, V_{DS}=0V, f=1MHz

Body Diode Characteristic

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Body Diode Forward Voltage	V_{SD}	-	-	1.2	V	V_{GS}=0V,I_{SD}=30A
Body Diode Continuous Forward Current	Is	-	-	54	A	TC = 25°C
Body Diode Pulsed Current	Is pulse	-	-	216	A	TC = 25°C
Body Diode Reverse Recovery Time	t_{rr}	-	17	-	ns	I_F=50A, dI/dt=100A/μs
Body Diode Reverse Recovery Charge	Q_{rr}	-	3.4	-	nC	

Typical Performance Characteristics

Fig 1: Output Characteristics

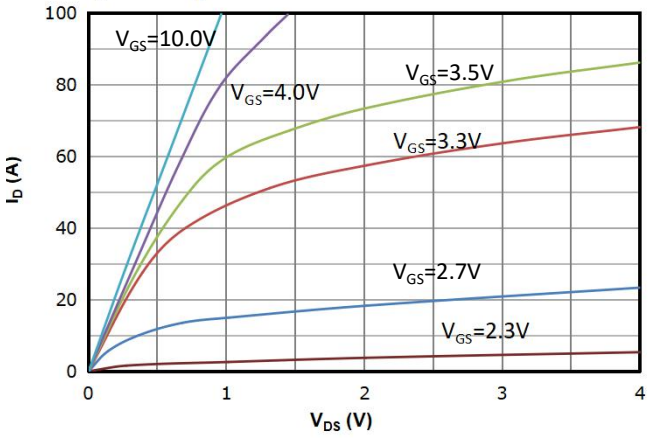


Fig 2: Transfer Characteristics

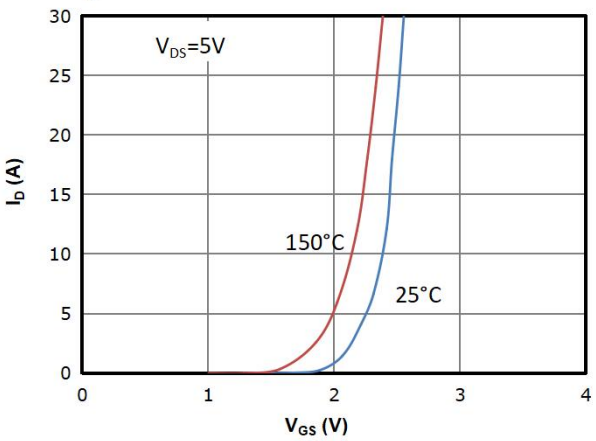


Fig 3: Rds(on) vs Drain Current and Gate Voltage

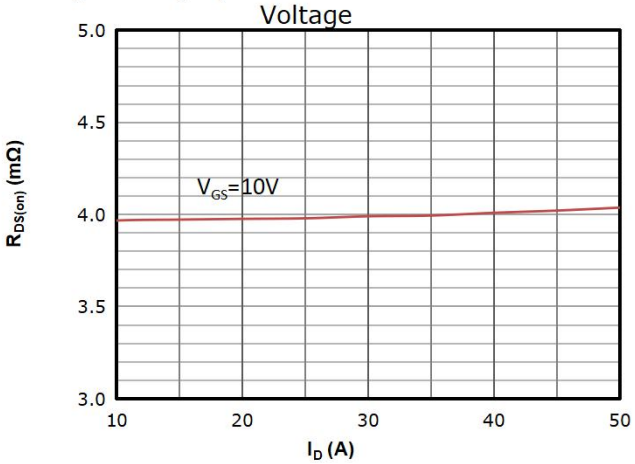


Fig 4: Rds(on) vs Gate Voltage

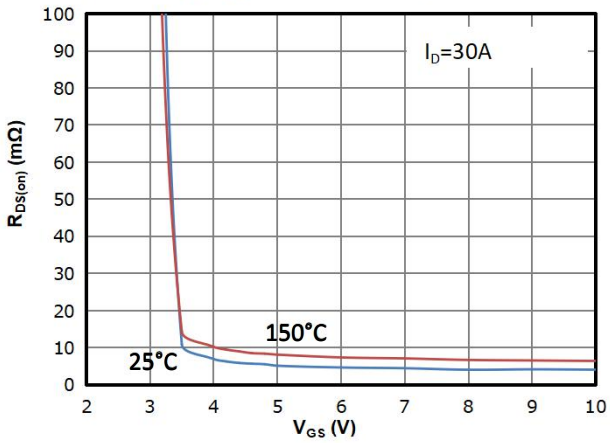


Fig 5: Rds(on) vs. Temperature

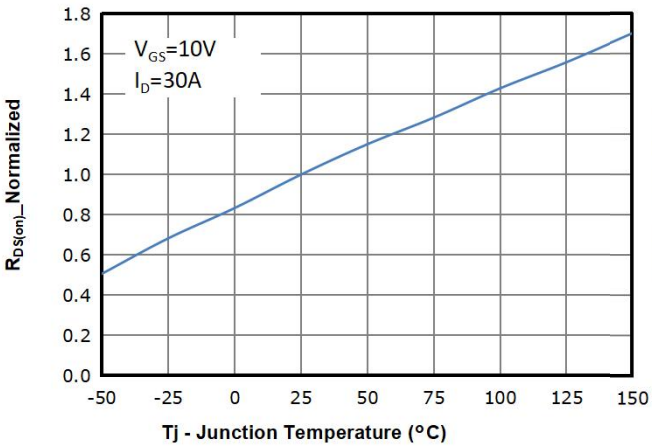


Fig 6: Vgs(th) vs. Temperature

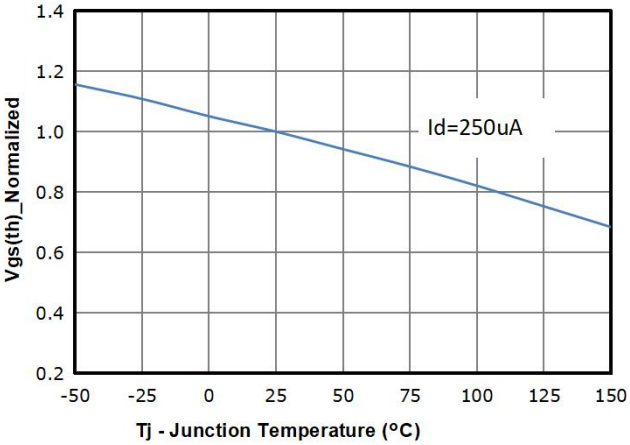


Fig 7: BVdss vs. Temperature

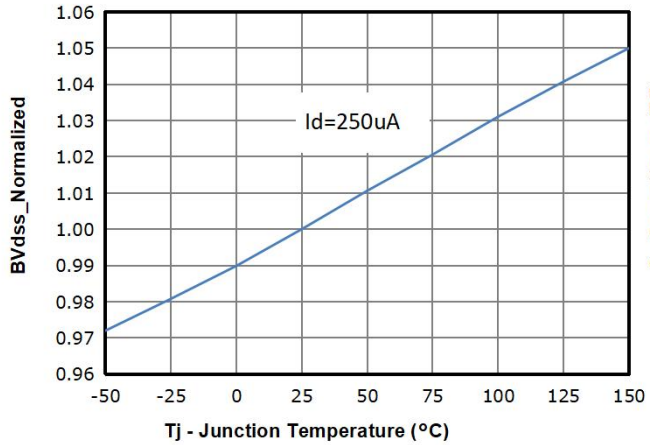


Fig 8: Capacitance Characteristics

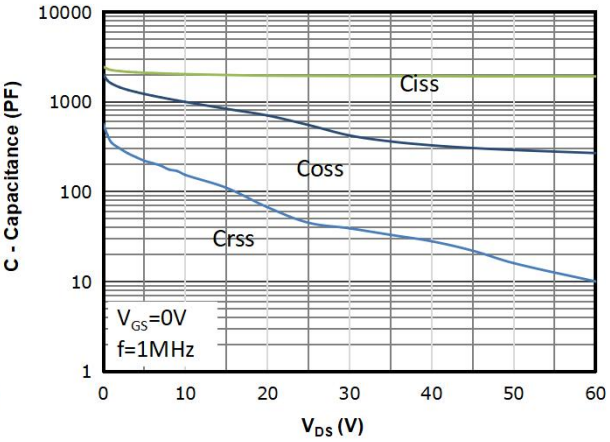


Fig 9: Gate ChargeCharacteristics

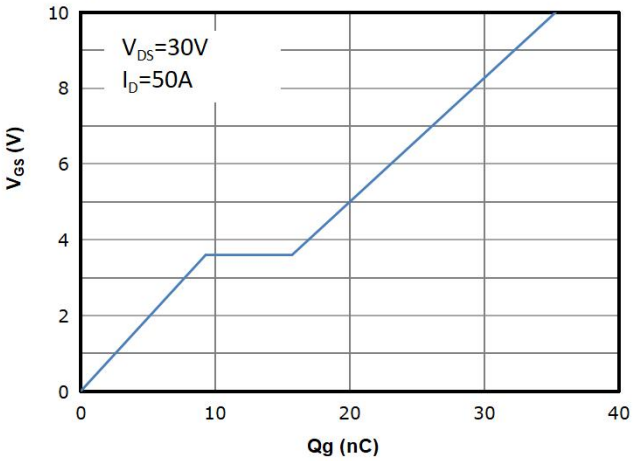


Fig 10: Body-diode Forward Characteristics

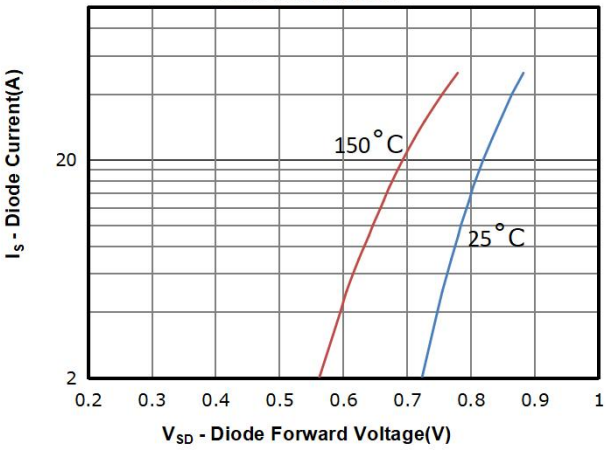


Fig 11: Power Dissipation

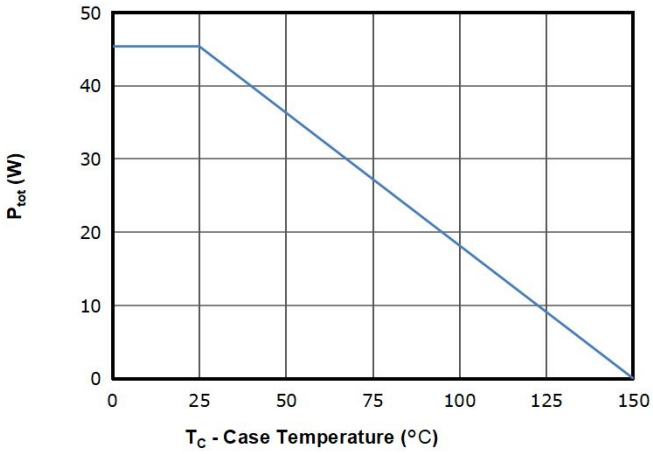


Fig 12: Drain Current Derating

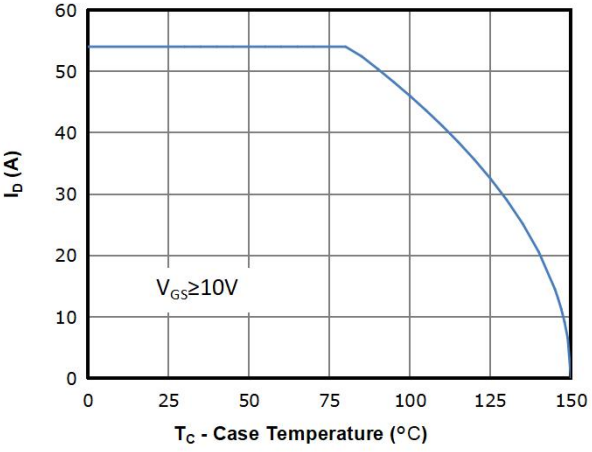


Fig 13: Safe Operating Area

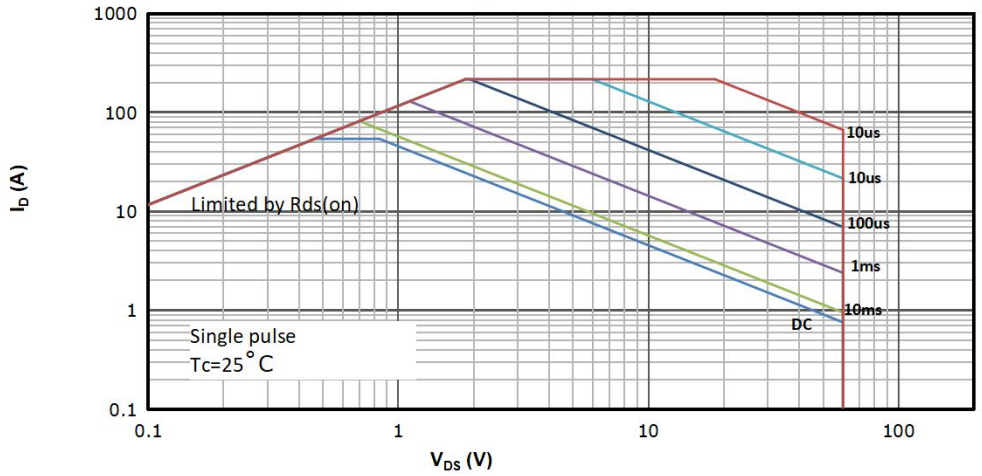
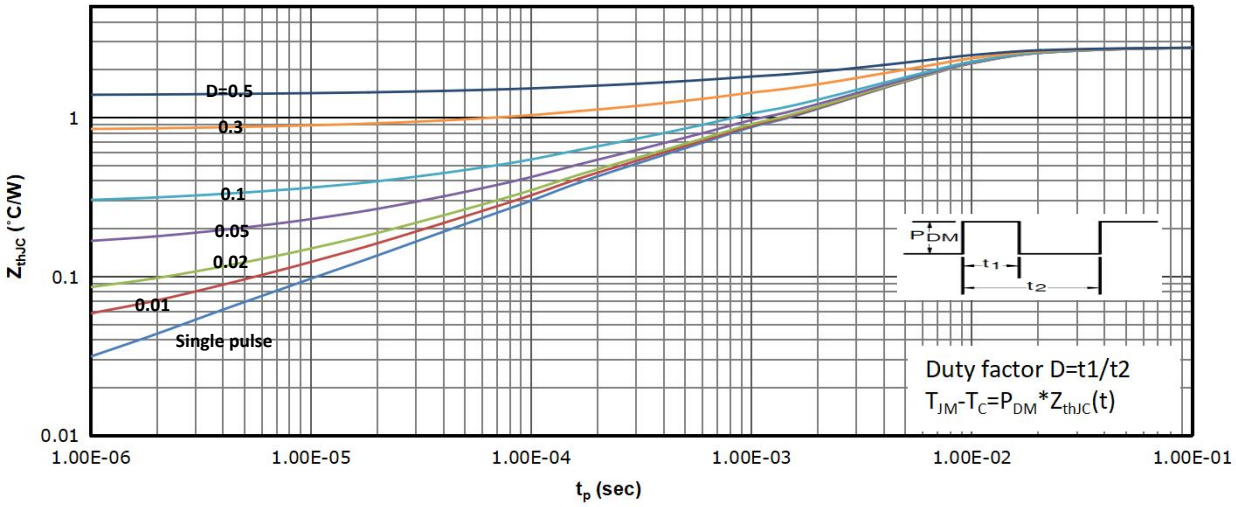
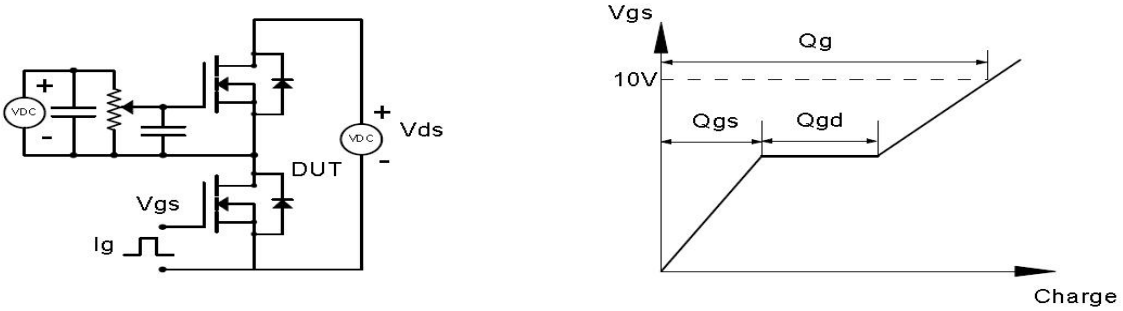


Fig 14: Max. Transient Thermal Impedance

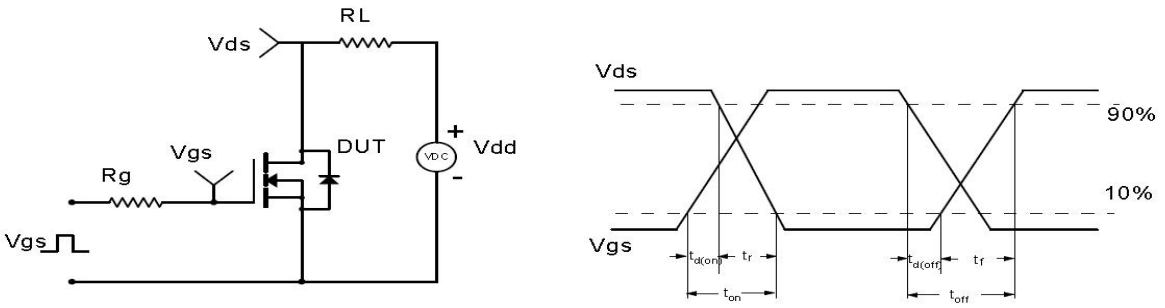


Test Circuit & Waveform

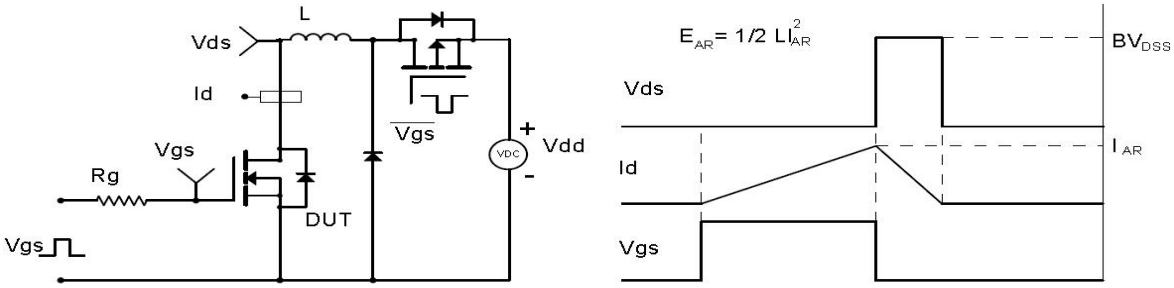
Gate Charge Test Circuit & Waveform



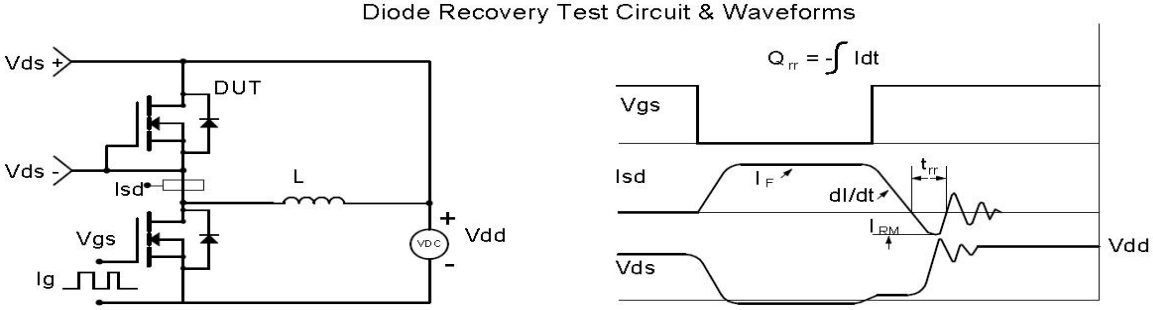
Resistive Switching Test Circuit & Waveforms



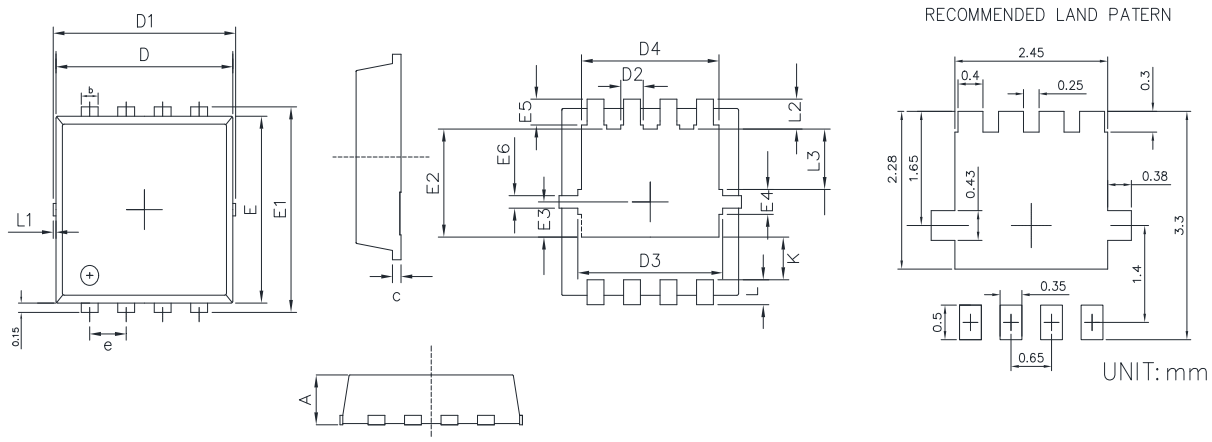
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Package Outline: DFN3X3



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.70	1.00	0.028	0.039
b	0.24	0.40	0.009	0.016
c	0.10	0.25	0.004	0.010
D	3.00	3.25	0.118	0.128
D1	3.10	3.50	0.122	0.138
D2	0.30	0.50	0.012	0.020
D3	2.50	2.70	0.098	0.106
D4	2.35	2.55	0.093	0.100
E	2.90	3.10	0.114	0.122
E1	3.15	3.45	0.124	0.136
E2	1.65	1.85	0.065	0.073
E3	0.48	0.68	0.019	0.027
E4	0.23	0.50	0.009	0.020
E5	0.20	0.40	0.008	0.016
E6	0.08	0.25	0.003	0.010
e	0.55	0.75	0.022	0.030
K	0.52	0.82	0.020	0.032
L	0.25	0.55	0.010	0.022
L1	0.00	0.10	0.000	0.004
L2	0.28	0.58	0.011	0.023
L3	0.88	1.08	0.035	0.043

Revision History

Revison	Date	Major changes
1.0	2023/9/7	Release of Formal Version.

Disclaimer

Any and all semicondutor products have certain probability to fail or malfunction, which may result in personal injury, death or property damage. Customer are solely responsible for providing adequate safe measures when design their systems.

Unless otherwise specified in the datasheet, the product is designed and qulified as a standard commercial product and is not intended for use in applications that require extraordinary levels of quality and reliability, such as automotive, aviation/aerospace and life-support devices or systems.

Buyer is responsible for its products and applications using PingWei products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by PingWei.

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